IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of:	Natsuo AJIKA	Group Art Unit:	Unassigned
Serial Number:	10/598,853	Examiner:	Unassigned
Filing Date:	September 13, 2006	Confirmation No.:	1312
For:	NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR WRITING THEREIN		

Preliminary Amendment Under 37 C.F.R. 1.115

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request entry and consideration of the attached amendments to the claims in the above listed application.

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper; and

Remarks begin on page 7 of this paper.

In The Claims:

This list of claims will replace all prior versions and listings of claims in the application. Please amend the claims as set forth below.

1. (Currently Amended) A method for programming bit data to a nonvolatile semiconductor memory device, said nonvolatile semiconductor memory device comprising,

an n type well formed in a semiconductor substrate,

a source and a drain of p+ regions formed in the surface of said n type well with a predetermined interval,

a channel region formed between said source and said drain,

a charge accumulation layer of a floating gate, a nano-crystal layer, a nonconductive charge trap layer ~~such as a silicon nitride layer, and so on,~~ formed above said channel region via a tunnel insulating layer, and

a gate electrode formed above said charge accumulation layer via an insulating layer,

said method comprising:

applying Vg, Vsub, Vs and Vd to the gate electrode, the n type well, the source and the drain respectively during programming, the Vg, the Vsub, the Vs and the Vd being in a relationship of "Vg>Vsub>Vs>Vd" and "Vg-Vd" being not less than an electrical potential difference necessary to generate a band to band tunneling current at said channel region,

thereby generating hot electrons near the drain by band to band tunneling[[,]]; and

injecting said hot electrons into said charge accumulation layer to program the bit data.

2. (Currently Amended) A method for programming bit data to a nonvolatile semiconductor memory device, said nonvolatile semiconductor memory device comprising,

a p type well formed in a semiconductor substrate,

a source and a drain of n+ regions formed in the surface of said p type well with a predetermined interval,

a channel region formed between said source and said drain,

a charge accumulation layer of a floating gate, a nano-crystal layer, a nonconductive charge trap layer ~~such as a silicon nitride layer, and so on,~~ formed above said channel region via tunnel insulating layer, and

a gate electrode formed above said charge accumulation layer via an insulating layer,

said method comprising[[,]]:

applying Vg, Vsub, Vs, and Vd to the gate electrode, the p type well, the source and the drain respectively during programming, the Vg, the Vsub, the Vs, and the Vd being in a relationship of "Vg<Vsub<Vs<Vd" and "Vd-Vg" being not less than an electrical potential difference necessary to generate a band to band tunneling current at said channel region[[,]];

thereby generating hot holes near the drain by band to band tunneling[[,]]; and

injecting said hot holes into said charge accumulation layer to program the bit data.

3. (Currently Amended) [[A]] The method for programming to a nonvolatile semiconductor memory device according to claim 1 ~~or claim 2~~, wherein two of the voltages from said Vg, Vsub, Vs and Vd are supplied from an external power supply.

4. (Currently Amended) [[A]] The method for programming to a nonvolatile semiconductor memory device according to claim 1 ~~or claim 2~~, wherein at least the Vd among said Vg, Vsub, Vs and Vd is supplied from an external power supply.

5. (Currently Amended) [[A]] The method for programming to a nonvolatile semiconductor memory device according to claim 1 ~~or claim 2~~, wherein the Vs and the Vd among said Vg, Vsub, Vs and Vd are supplied from an external power supply.

6. (Currently Amended) [[A]] The method for programming to a nonvolatile semiconductor memory device according to claim 5, wherein said Vs is a power supply voltage and the Vd is a ground voltage.

7. (Currently Amended) A nonvolatile semiconductor memory device, comprising:

an n type well formed in a semiconductor substrate;

a source and a drain of p+ regions formed in the surface of said n type well with a predetermined interval;

a channel region formed between said source and said drain;

a charge accumulation layer of a floating gate, a nano-crystal layer, a nonconductive charge trap layer formed above said channel region via a tunnel insulating layer; and

a gate electrode formed above said charge accumulation layer via an insulating layer,

wherein [[having]] memory cells of said memory device are programmed by: ~~the method of claim 1 or claim 2,~~

applying Vg, Vsub, Vs and Vd to the gate electrode, the n type well, the source and the drain respectively during programming, the Vg, the Vsub, the Vs and the Vd being in a relationship of "Vg>Vsub>Vs>Vd" and "Vg-Vd" being not

less than an electrical potential difference necessary to generate a band to band tunneling current at said channel region,

thereby generating hot electrons near the drain by band to band tunneling; and

injecting said hot electrons into said charge accumulation layer to program the bit data, and

wherein the memory cells are arrayed by connecting in a NOR type or in a NAND type circuit.

8. (New) The method for programming to a nonvolatile semiconductor memory device according to claim 2, wherein two of the voltages from said Vg, Vsub, Vs and Vd are supplied from an external power supply.

9. (New) The method for programming to a nonvolatile semiconductor memory device according to claim 2, wherein at least the Vd among said Vg, Vsub, Vs and Vd is supplied from an external power supply.

10. (New) The method for programming to a nonvolatile semiconductor memory device according to claim 2, wherein the Vs and the Vd among said Vg, Vsub, Vs and Vd are supplied from an external power supply.

11. (New) The method for programming to a nonvolatile semiconductor memory device according to claim 10, wherein said Vs is a power supply voltage and the Vd is a ground voltage.

12. (New) A nonvolatile semiconductor memory device comprising:

a p type well formed in a semiconductor substrate;

a source and a drain of n+ regions formed in the surface of said p type well with a predetermined interval;

a channel region formed between said source and said drain;

a charge accumulation layer of a floating gate, a nano-crystal layer, a nonconductive charge trap layer formed above said channel region via tunnel insulating layer, and;

a gate electrode formed above said charge accumulation layer via an insulating layer,

wherein memory cells of said memory device are programmed by

applying Vg, Vsub, Vs, and Vd to the gate electrode, the p type well, the source and the drain respectively during programming, the Vg, the Vsub, the Vs, and the Vd being in a relationship of "Vg<Vsub<Vs<Vd" and "Vd-Vg" being not less than an electrical potential difference necessary to generate a band to band tunneling current at said channel region,

thereby generating hot holes near the drain by band to band tunneling, and

injecting said hot holes into said charge accumulation layer to program the bit data, and

wherein the memory cells are arrayed by connecting in a NOR type or in a NAND type circuit.

REMARKS

This Preliminary Amendment presents the claims in proper format for examination in the United States. No new matter is added by the amendments or new claims.

The Examiner is invited to contact the undersigned for any reason related to the advancement of this case.

Respectfully submitted,

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